Page 39, first paragraph, replace with the following:

Step (d-4): the syndrome calculator 5 performs error-containing code detection for every transferred code word, and outputs the syndrome 16 to the error corrector 6. When an error-containing code word is detected, the syndrome calculator 5 outputs the error-containing code detection signal 22 to the error detector 7 and to the DMA control unit 2. On the other hand, the error detector 7 also executes error detection for each code word. Only when the error-containing code detection signal 22 has not been outputted, the mid-term results of error detection for each code word are stored in the mid-term result register 8. When the detection of error-containing code has been informed by the error-containing code detection signal 22, the error detector 7 suspends an error detecting process. At the same time, the syndrome calculator 5 informs the DMA control unit 2 of the detection of an error-containing code. The DMA control unit 2 suspends an output of the DMA request 13 to the bus control unit 3. The bus control unit 3 suspends a data transfer from the buffer memory 4 to the syndrome calculator 5.

Page 45, fourth paragraph, replace with the following:

Step (e-2): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Page 47, third full paragraph, replace with the following:

Step (e-9): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read the data therefrom. Then, the bus control unit 3 outputs the error detector data supply signal 20 to the error detector 7 so as to supply the data read from the buffer memory 4.

Page 54, fourth paragraph, replace with the following:

Step (f-12): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector 6 and writes the data to the buffer memory 4.

Page 56, first full paragraph through third paragraph, replace with the following:

Step (f-13): in order to execute the third-time error correction for the third ECC block, the system control unit 1 outputs the DMA command 12 to the DMA control unit 2 so as to provide instructions to transfer data corresponding to a horizontal code word in the third ECC block from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (f-14): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

a6

Step (f-15): the bus control unit 3 puts the data bus 11 in commission, and outputs the buffer memory access signal 14 to the buffer memory 4 to read data therefrom. The bus control unit 3 then outputs the syndrome data supply signal 15 and the error detector data supply signal 20 to the syndrome calculator 5 and the error detector 7, respectively, so as to supply the data read from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Page 57, first, second and third paragraphs, replace with the following:

Step (f-16): the syndrome calculator 5 calculates a syndrome 16 of the transferred horizontal code word, and outputs the syndrome 16 to the error corrector 6. If the code word contains an error-containing code or if the syndrome is not zero, the syndrome calculator 5 outputs the error-containing code detection signal 22 to the error detector 7 and to the system control unit 1. The syndrome calculator 5 also provides the system control unit 1 with the error-containing code word signal 23 indicating the code word from which an error has been detected.

a7

The error detector 7 executes an error detecting process for the transferred data in parallel with the syndrome calculator 5. Prior to the error detection, the mid-term results of the EDCs in the preceding code words stored in the third mid-term result registers 83 are reloaded. If the syndrome is zero when the transfer of the code words is over, the mid-term results of the EDCs are stored in the third mid-term result register 83 again. When the syndrome is not zero, on the other hand, the mid-term results of the EDCs in the preceding code words are maintained,

without updating the contents of the third mid-term result register 83. In the first horizontal code word, the third mid-term result register 83 holds the mid-term results obtained in the first-time error correction. If the detection of an error is informed by the error-containing code detection signal 22, the subsequent code words are not subjected to error detection.

a7

Step (f-17): the error corrector 6 corrects an error in the code, and transmits the access request signal 17 to the bus control unit 3 to request writing of the error-corrected data to the buffer memory 4.

Page 57, fourth paragraph through Page 58, fourth paragraph, replace with the following:

Step (f-18): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector 6 and writes them to the buffer memory 4.

a8

Step (f-19): the system control unit 1 outputs the DMA command 12 to the DMA control unit 2 in order to check to see that the error-corrected data contain no error, and provides instructions for data transfer from the buffer memory 4 to the error detector 7.

This data transfer involves data from the code word indicated by the error-containing code word signal 23 outputted together with the error-containing code detection signal 22 outputted first by the syndrome calculator 5 at step (f-4).

Step (f-20): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the error detector 7.

Step (f-21): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read the data therefrom. Then, the bus control unit 3 outputs the error detector data supply signal 20 to the error detector 7 so as to supply the data read from the buffer memory 4.

Step (f-22): using the mid-term results of the error detection stored in the third mid-term register 83, the error detector 7 executes error detection of the transferred subsequent data, and transmits the error detection signal 21 to the system control unit 1 so as to inform whether an error has been detected or not.

Page 62, fourth paragraph through Page 63, second paragraph, replace with the following:

In order to perform error correction and error detection with the code word read from the buffer memory 4, the first syndrome calculator 51 and the first error detector 71 are arranged separately. The input of the error corrector 6 is connected to a selection circuit 60 so that the error corrector 6 can select between the syndromes transmitted from the first and second syndrome calculators 51 and 52.

a 9

The second syndrome calculator 52 calculates a syndrome 162 of each transferred horizontal code word, and outputs the syndrome 162 to the error corrector 6. If the code word contains an error-containing code or if the syndrome 162 is not zero, the second syndrome calculator 52 outputs the error-containing code detection signal 222 to the second error corrector 72 and to the system control unit 1. The second syndrome calculator 52 also provides the system control unit 1 with an error-containing code word signal 232 indicating the code word from which an error has been detected.